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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,877	10/02/2003	Taiji Noda	60188-670	8100

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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,877	NODA, TAIJI	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *15-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/03/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's amendment filed on October 03, 2005. Claims 1-18 are pending, in which claim 18 has been newly added, and in which claims 15-17 are non-elected without traverse as treated.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

1. Claims 1-3,6-7,9,18 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (2001/0041432).

Lee teaches a method for forming a semiconductor device comprising at least the steps of: a first step of implanting, into a channel formation region of a semiconductor substrate 12, first dopant ions of a first conductivity type of ions, which are heavy ions with a relatively large mass number, to form a dopant implantation layer in the channel formation region (Figs 2a,2e,2a,2d; paragraphs 45-48 or paragraphs 42-44); a second step of implanting a second dopant ions into the semiconductor substrate to form an amorphous layer expanding from the substrate surface to a region of the substrate deeper than the dopant implantation layer (paragraphs 42-44,48 or paragraphs 50-51); after the first and second steps, a third step of performing a first thermal treatment (paragraph 54-56) to diffuse the first dopant ions (paragraphs 45-48 or paragraphs 42-44) from the dopant implantation layer thereby forming a first diffused layer of the first conductivity type in the channel formation region 24 (Fig 2d); and after the third step, a fourth step of selectively forming a gate insulating film on the semiconductor substrate and a gate electrode on the gate insulating film (Figs 2d,2e,5; paragraph 40; paragraph 57-60; Fig 2d,2b,5). Re claim 2 , wherein the semiconductor substrate 12 is made of silicon (paragraph 36) , and the second dopant ion of germanium belongs to group IV elements (paragraphs 50-51 or paragraph 42). Re claim 3, wherein the semiconductor substrate is {100} plane (paragraph 0062). Re claim 6, wherein the heavy ions are indium ions (paragraph 42). Re claim 7, wherein the dose of the heavy ions of indium to be implanted includes $1x\ 10^{14}/cm^2$ to $1x\ 10^{15}/cm^2$ (paragraph 43). Re claim 9, wherein the first heat treatment is RTA at a temperature of 850-1100°C at a rate of 50-500°C/sec and keep at about 5 seconds (paragraph 54-56). Re claim 18, wherein the first and second steps are carried out in any order (paragraph 48).

Claim Rejections - 35 USC § 103

2. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (2001/0041432) taken with Sundaresan (6,190,179).

Lee teaches a method for forming a semiconductor device as applied to claims 1-3,6-7,9 above.

Lee lacks growing an epitaxial silicon on the semiconductor substrate.

However, Sundaresan teaches (at Figs 1-4; col 2, lines 16-64; col 3, lines 8-25) the desirability of growing an epitaxial silicon 16 on a semiconductor substrate 10.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a semiconductor device of Lee by growing an epitaxial silicon on the semiconductor substrate as taught by Sundaresan. This is because of the desirability to form a reliable semiconductor device having good operating characteristics with a minimal degradation form short channel effects.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (2001/0041432 taken with Sonoda (6,696,341).

Lee teaches a method for forming a semiconductor device as applied to claims 1-3,6-7,9 above.

Lee lacks having a strained silicon layer having a crystal lattice of a larger lattice constant than a normal lattice constant on the semiconductor substrate.

However, Sonoda teaches forming a strained silicon layer 3 having a crystal lattice of a larger lattice constant than a normal lattice constant on the semiconductor substrate 2/1 (Fig 1, col 8, line 58 through col 9)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a semiconductor device of Lee by forming a strained silicon layer having a crystal lattice of a larger lattice constant than a normal lattice constant on the semiconductor substrate as taught by Sonoda. This is because of the desirability to reduce breakdown field so as to improve ESD resistance and protection of the semiconductor device.

4. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (2001/0041432) taken with Wang et al (6,368,928).

Lee teaches a method for forming a semiconductor device as applied to claims 1-3,6-7,9 above.

Re claim 10 Lee lacks, between the second and third steps, performing a third thermal treatment at such a temperature of so that the first dopant ions do not diffuse from the dopant implantation layer and that the crystallinity of the amorphous layer is restored, thereby recovering crystal damages caused by the first dopant ions, wherein the temperature is 400 to 600°C (re claim 11) for a time of 1 to 20 hours (re claim 12).

However, Wang teaches (at col 4, lines 6-31) after implanting the dopant ions, performing a third thermal treatment at such a low temperature of 450-650°C for a time of up to 3 hours (180 minutes) so that the first dopant ions do not diffuse from the dopant implantation layer and that the crystallinity of the amorphous layer is restored, thereby recovering crystal damages caused by the first dopant ions.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a semiconductor device of Lee by performing a third thermal treatment at such a low temperature of 450-650°C for a time of up to 3 hours, as taught by Wang. This is at least because of the desirability to recover crystal damage and limiting diffusion of the implanted dopant ions so that the first dopant ions do not diffuse from the dopant implantation layer and that the crystallinity of the amorphous layer is restored, thereby recovering crystal damages caused by the first dopant ions.

5. Claims 8,13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (2001/0041432) taken with Noda et al (6,432,802).

Lee teaches a method for forming a semiconductor device as applied to claims 1-3,6-7,9 above. Re claim 8, after the fourth step, a fifth step of implanting third dopant ions of a second conductivity type into the semiconductor substrate using the gate electrode as a mask (Figs 2b-2e, 2d; paragraphs 36-49; Fig 5, paragraph 60), wherein a thermal treatment is performed on the semiconductor substrate to diffuse the third dopant ions (paragraphs 54-56) thereby forming a

second diffused layer as source and drain of the second conductivity type whose junction position is relatively shallow (Figs 2b-2e;5).

Re claims 8,13-14; Lee lacks implanting third, fourth, and fifth dopant ions using the gate electrode as a mask, and performing a thermal treatment after each implantation to form diffuse layers.

However, Noda teaches to form a LDD MOS device having lightly doped source/drain by implanting third, fourth, and fifth dopant ions using the gate electrode as a mask, and sidewalls spacer, and performing a thermal treatment after each implantation in order to diffuse and form diffuse layers. Specifically, Re claim 8, Noda teaches, after the fourth step, a fifth step of implanting third dopant ions of a second conductivity type into the semiconductor substrate using the gate electrode as a mask (Figs 5b-5d; col 12, lines 12-34), and a sixth step of performing a second thermal treatment on the semiconductor substrate to diffuse the third dopant ions, thereby forming a second diffused layer 305A of the second conductivity type whose junction position is relatively shallow (Figs 5b-5d; col 12, lines 56-65). Re claim 13, Noda teaches, between fourth and six steps, implanting fourth dopant ions of the first conductivity type using the gate electrode 302 as a mask, where the second heat treatment performed in the six steps diffuses the fourth dopant ions to form a third diffused layer 306 of the first conductivity type below the second diffused layer 305 (Figs 5B-5D,6A; col 12, lines 18-34; and lines 56-67). Re claim 14, Noda teaches, after the six step, forming sidewalls 307 of an insulating film on the side surfaces of the gate electrode 302 (Fig 6B; col 13, lines 1-7), and implanting fifth dopant ions of the second conductivity type using the gate electrode 302 and the sidewalls 307 as a mask, then fourth heat treatment to diffuse fifth dopant layer, thereby forming, outside the second diffused layer 305, a fourth diffused layer 304 of the second conductivity type which has a deeper junction interface than the second diffused layer 305 (Figs 6b-6c; col 13, lines 8-18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a semiconductor device of Lee by implanting third, fourth, and fifth dopant ions using the gate electrode as a mask, and sidewall, and performing a thermal treatment after each implantation to form diffuse layers, as above taught by Noda. This is because of the desirability to activate and diffuse the implanted dopant ions, and to form a LDD MOS device

having shallow source and drain regions that can operate at a high speed with reduced leakage current.

Response to Amendment

6. Applicant's remarks filed October 03, 2005 with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

*** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272- 1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number is (571) 273-8300

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.
Oacs-16

Michael Trinh
Primary Examiner